IN THE CLAIMS

Please amend claims 22, 50, 55-57 as follows below.

This marked up listing of claims replaces all prior versions, and listings, of claims in the application:

Marked-Up Listing of Claims:

1-19. (Cancelled)

20. (Previously Presented) A bus state keeper comprising:

a plurality of multiplexers each having

a select input,

a first input,

a second input, and

an output,

the output coupled to each respective bit of a first bus coupled to a plurality of devices, wherein the first bus is to be kept in a steady state when inactive,

the first input coupled to each respective bit of a second bus,

the select input of each of the plurality of multiplexers coupled to a select signal;

and

a plurality of flip flops each having

a data input,

a data output,

a clock input,

the data input coupled to each respective bit of the first bus,

the data output coupled respectively to the second input of the plurality of multiplexers,

the clock input coupled to a clock signal, and

the plurality of flip flops to store a state of the first bus in response to the select signal.

21. (Original) The bus state keeper of claim 20, wherein,

the plurality of flip flops are clocked by the clock signal to store a state of the first bus.

22. (Currently Amended) The bus state keeper of claim 20, wherein,

the select signal input to each select input of the plurality of multiplexers selects between

outputting ~~from the plurality of multiplexers~~ a stored state in the flip flops onto the first bus

or

outputting the state of the second bus onto the first bus.

23. (Previously presented) The bus state keeper of claim 20, wherein,

the select signal input to each select input of the plurality of multiplexers selects to output from the plurality of multiplexers a stored state in the flip flops onto the first bus to maintain a state of the first bus.

24. (Original) The bus state keeper of claim 23, wherein,

the select signal maintains a state of the first bus to conserve power.

25-39. (Cancelled)

40. (Previously presented) A bus state keeper for conserving power, the bus state keeper comprising:

a plurality of flip flops to store a state of an output bus, the output bus having a plurality of bits, each of the plurality of flip flops having

a data input,

a data output,

a clock input, and

wherein the data input of each flip flop is coupled to a respective bit of the output bus, and

the clock input of each is coupled to a clock signal; and,

a plurality of multiplexers coupled to the plurality of flip flops, an input bus, and the output bus coupled to a plurality of devices, each of the plurality of multiplexers having

a select input,

a first input,

a second input, and

an output,

wherein the select input of each multiplexer is coupled to a select signal,

the first input of each multiplexer is coupled to a respective bit of the input bus,

the second input of each multiplexer is coupled to the data output of a respective flip flop, and

the output of each multiplexer is coupled to a respective bit of the output bus.

41. (Previously presented) The bus state keeper of claim 40, wherein, the plurality of flip flops are clocked by the clock signal to store a state of the output bus.

42. (Previously presented) The bus state keeper of claim 40, wherein,

each of the plurality of flip flops are a single bit D type flip flop.

43. (Previously presented) The bus state keeper of claim 40, wherein, when the output bus is selected to be output by the plurality of multiplexers, the bus state keeper recycles the state of the output bus to keep it in a steady state and conserve power.

44. (Previously presented) The bus state keeper of claim 40, wherein,

when the input bus is selected to be output by the plurality of multiplexers,

the bus state keeper drives the state of the input bus onto the output bus to change the state of the output bus.

45. (Previously Presented) A bus state keeper to couple

between an input bus and an output bus, the bus state keeper comprising:

a bus multiplexer selectively coupled between a first bus input or a second bus input and a bus output in response to a select input, the bus multiplexer including a plurality of single bit multiplexers, and wherein

the select input of the bus multiplexer is coupled to a select signal,

the first bus input of the bus multiplexer is coupled to the input bus, and

the bus output of the bus multiplexer is coupled to the output bus, the output bus coupled to a plurality devices;

and

a bus register to store a state of a data bus input and output the state at a data bus output in response to a clock input, the bus register including a plurality of single bit flip flops, and wherein

the data bus input of the bus register is coupled to the output bus,

the data bus output of the bus register is coupled to the second bus input of the bus multiplexer, and

the clock input coupled to a clock signal.

46. (Previously presented) The bus state keeper of claim 45, wherein,

the bus register is clocked by the clock signal to store a state of the output bus.

47. (Previously presented) The bus state keeper of claim

45, wherein,

the plurality of single bit flip flops of the bus register are D type flip flops.

48. (Previously presented) The bus state keeper of claim 45, wherein,

when the second bus input of the bus multiplexer is selected to be coupled onto the bus output by the bus multiplexer,

the bus state keeper to recycle the state of the output bus to keep it in a steady state and conserve power.

49. (Previously presented) The bus state keeper of claim 45, wherein,

when the first bus input of the bus multiplexer is selected to be coupled onto the bus output by the bus multiplexer,

the bus state keeper to drive the state of the input bus onto the output bus to change the state of the output bus.

50. (Currently Amended) A bus state keeper for conserving power, the bus state keeper comprising:

a plurality of bit bus keepers coupled between bits of an input bus and bits of an output bus, the plurality of bit bus keepers to store a state of the bits of the output bus, each of the plurality of bit bus keepers including

a flip flop to store a state of a respective bit of the output bus as a stored state, the flip flop having

a data input coupled to a respective bit of the output bus,

a data output,

a clock input coupled to a clock signal,

the flip flop adapted to store the state of the data input in response to the clock input;

and,

a multiplexer coupled to the flip flop, the multiplexer to couple to a respective bit of the input bus and the respective bit of the output bus, the respective bit of the output bus coupled to a plurality of devices, the multiplexer having

a select input coupled to a select signal,

a first input coupled to the respective bit of the input bus,

a second input coupled to the data output of the flip flop, and

an output coupled to the respective bit of the output bus, and

the multiplexer adapted to selectively drive the respective bit of the output bus with

a state of the respective bit of the input bus to change the state of the respective bit of the output bus

or

the stored state of the respective bit of the output bus to maintain the state of the respective bit of the output bus.

51. (Previously presented) The bus state keeper of claim 50, wherein,

the flip flop of each of the plurality of bit bus keepers is a D type flip flop.

52. (Previously presented) The bus state keeper of claim 50, wherein,

the bus state keeper to recycle the state of the bits of the output bus to keep it in a steady state and conserve power in response to the select signal.

53. (Previously Presented) The bus state keeper of claim 20, wherein,

one of the plurality of devices coupled to the first bus is a flip flop of the plurality of flip flops.

54. (Previously Presented) The bus state keeper of claim 20, wherein,

another one of the plurality of devices coupled to the first bus is a memory block.

55. (Currently Amended) The bus state keeper of claim 40, wherein,

one of the plurality of devices coupled to the [[first]] output bus is a flip flop of the plurality of flip flops.

56. (Currently Amended) The bus state keeper of claim 45, wherein,

one of the plurality of devices coupled to the [[first]] output bus is a flip flop of the plurality of flip flops.

57. (Currently Amended) The bus state keeper of claim 50, wherein,

one of the plurality of devices coupled to the [[first]] respective bit of the output bus is the flip flop.